COMMENTARY

A guide for nanowire growth

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Human fascination with growth has been around since the Neolithic Revolution began more than 10 millennia ago. With it grew the science and understanding behind the underlying mechanisms found in nature, which are often applied toward practical benefits such as bigger produce or higher yields. For example, farmers plant seeds in specific and optimally spaced positions that allow dense and organized fields to develop (Fig. 1*A*), whereas villagers in Cherrapunjee, India, grow tree roots across rivers to form living bridges. Other aesthetic applications include guided growth of vines over an arbor (Fig. 1*B*) or even living sculptures and "tree shaping" (Fig. 1*C*). The same underlying principles apply to nanowires: guiding growth using catalyst seeds along a template, as developed by Schvartzman et al. and presented in PNAS (1). At the nanoscale, this becomes an indispensable tool for synthesizing the precisely ordered patterns required by advanced electronic applications. Nature is often a model to mimic (2, 3) but is also a barrier that technology must overcome; ultimately, it can be tamed by exploiting these forces through engineering to produce bountiful results.

At the crux of advanced electronic fabrication is the intersection of top-down and bottom-up approaches toward building nanostructures for practical functionality in an economical way. Living organisms are the original bottom-up assemblers: multitudinous nanoscopic pieces (proteins, DNA, etc.) work together to make microscopic machines (cells) that self-replicate and assemble together to form all kinds of life. On the other hand, top-down is a crude tactic not generally found in nature: we cut down trees, grind down stones into tools, and use otherwise blunt subtraction to create a desired product. In terms of horticulture, this is analogous to pruning or cutting away branches, in contrast to training and directed growth. The electronics industry has been dominated by top-down fabrication methods of traditional semiconductor technologies; however, bottom-up growth is seen as an inevitable necessity to breach the limits of conventional lithography (4, 5). Nanotechnology has seen a convergence of these two strategies, cherry picking the advantages of either to realize novel architecture design at scales beyond the capabilities of one technique on its own.

Nanowires like to grow in a similar fashion to trees: straight up. The recent development of the vapor-liquid-solid (VLS) growth method has propelled the field to new heights, where a nanoscale liquid drop of catalyst facilitates the (typically) vertical growth of high-quality, solid nanowires using vapor phase reagents (Fig. 1*D*) (6). However, vertical nanowires are not necessarily very practical for electronics, as most device structures and fabrication techniques require horizontal geometries. This is where guided growth becomes an essential method to dictate the orientation of a nanowire: with a precisely engineered system, they will grow along predefined geometries. Positioning the nanowires in a well-organized, dense array is critical in the fabrication of integrated circuits. Growing the nanowires directly into place for each device avoids any further alignment steps. Novel strategies for scalable and efficient synthesis of ordered nanowire arrays have been developed, such as nanoimprint lithography (7, 8) and post-growth assembly using mechanical (9, 10) or electromagnetic (11) forces and self-assembly (12). They have their advantages, but none achieve the same degree of alignment and control as guided growth.

Nanowire growth is influenced by its environment, just like trees tend to grow toward the most sunlight and vines wrap themselves around pillars. Many advanced technologies have used guided growth principles at microscopic scales, such as surface modifications and 3D scaffolds designed to guide cell growth and tissue engineering (13). Other 1D nanostructures have been synthesized using template surfaces, such as chemical vapor deposition growth of carbon nanotubes on quartz (14) and epitaxial growth of graphene nanoribbons on nanofaceted silicon carbide (15). A novel approach toward controlling nanowire growth uses substrates that are patterned with a template of nanoscale crystallographic surfaces. Such patterned facets

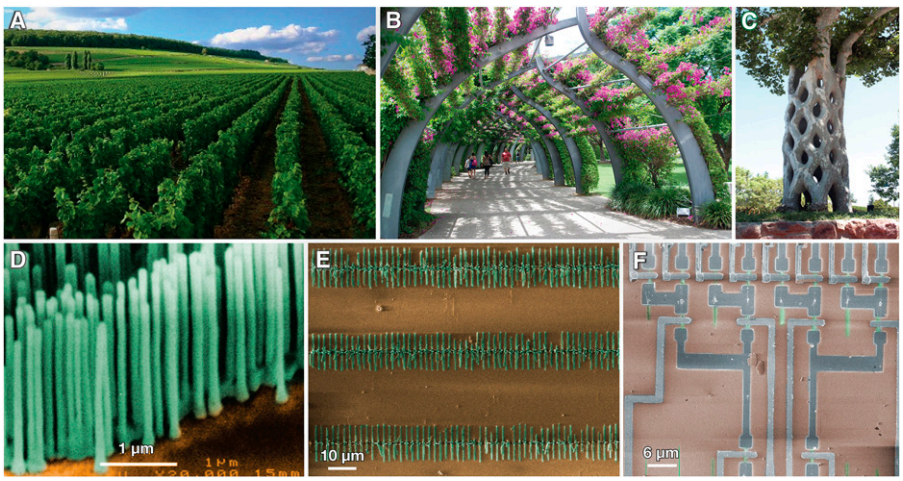

Fig. 1. Guided growth in nature and nanowires. (*A*) Vineyard: Farmers create linear patterns by planting seeds in precise locations. (*B*) Grand Arbor in South Bank Australia: Vines growing along a horizontal template. (*C*) "Basket Tree": The art of tree sculpture, a combination of guided growth, training, and grafting, is used to slowly manipulate the formations that trees can make. This piece of art was created by Axel Erlandson, completed in 1947, and is located in Gilroy Gardens, CA. (*D*) Tilted SEM images of vertically grown forest of VLS nanowires. (*E*) SEM image of guided horizontal growth on a crystal surface, showing highly parallel synthesis of precisely located nanowires with end-to-end registration. (*F*) This process enables direct integration of the nanowires into more complex circuits such as this SEM image of a three-bit address decode. Photos courtesy of and copyrighted by (*A*) Stefan Bauer, (*B*) Lee Mylne, and (*C*) Richard Reames. (*D*) Reproduced with permission from ref. 6 and copyrighted by the Association for the Advancement of Science 2001. (*E* and *F*) Reproduced from ref. 1.

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create an energetically preferred growth vector, allowing nanowires to only grow along the predefined channel. Seminal work by Melosh et al. (16) used perpendicular epitaxial growth on specific crystal facets, demonstrating reasonable scalability and extremely high precision. However, this approach is limited by the lithographically patterned top-down features and requires molecular beam epitaxy techniques that are typically more challenging and less practical than VLS growth strategies.

More recently, the Joselevich group developed a horizontal VLS growth method that yields high-quality nanowires that are parallel to the surface (17). Here, the crystallographic facets resemble tracks for the nanowires to extend down. Further progress is reported here in PNAS using ZnO nanowires on a $(1\bar{1}02)$ R-plane sapphire substrate (1). Because the orientation of the nanowire is defined by the crystallographic orientation of the substrate, it enables an unprecedented accuracy, with 99% of the nanowires aligned within ±0.1° (Fig. 1*E*), significantly better than state-of-the-art postgrowth assembly approaches (18). Furthermore, this technique attains precise lengths, as all of the nanowires grow at the same time and same rate, yielding length deviations less than 12%, a significant improvement over previous directed growth results.

In addition to incremental improvements in alignment and consistency, this work incorporates prepatterned gold nanoparticle catalysts that act as both the seeds to initiate the growth at precise locations and as the train engines that drive the growth along the track. Although the surface patterning defines the growth direction, the nanoparticle seed position determines the beginning location, and its size affects the nanowire diameter and growth rate. This innovation establishes a reliable method for directly positioning the ends of each nanowire with exceptional precision (Fig. 1*E*), with over half of the nanowires' lateral positions within ±50 nm from the initial seed position. Additionally, this approach is highly scalable and enables end-to-end "registration" of the nanowires (deterministic positioning of each end), which facilitates the alignment for device fabrication in subsequent lithography processes. The seed patterns can be matched to predefined circuit designs, integrating the top-down and bottom-up strategies, which makes this technique a promising candidate for incorporation into contemporary semiconductor technologies.

To demonstrate the feasibility of building integrated circuits using this guided growth approach, Schvartzman et al. perform a proof-of-concept array of more than100 top-gated transistors with a yield of 85%. They have further demonstrated a three-bit address decoder with 14 transistors integrated into a single circuit (Fig. 1*F*), illustrating the potential mass scalability of this technique.

Concurrently positioning nanowires during growth offers a number of clear advantages over postgrowth assembly techniques.

The improvements shown in this report make it a promising complementary route to microchip production. In particular, the deterministic positioning of nanowires in a parallel process allows for scalable direct integration with existing top-down manufacturing. However, these technologies are still in their early stages, and many obstacles remain before it becomes viable at any practical scale. To truly replace the dense circuitry of microelectronics, nanowires must be as thin and compact as possible. Ostwald ripening of the nanoparticle catalysts during dewetting of the gold thin film, as outlined in the article, causes variability in nanowire size and growth rate and limits the minimum size. This may prove to be a serious limitation, as the variability in performance, such as conductance and transconductance, will suffer greatly from a large distribution in nanowire size. Applications will also require the nanowire arrays to be patterned as densely and precisely as possible, whereas this VLS growth may be limited by surface diffusion mobility of the liquefied gold nanoparticles.

Concurrently positioning nanowires during growth offers a number of clear advantages over postgrowth assembly techniques that are unlikely to be outdone. However, inevitably, this approach comes with its own inherent drawbacks as well. For example, the particular substrate/nanowire material combination requirements can greatly limit compositional versatility. Further refinement of the process is still necessary to improve the consistency, precision, yield, and density of the grown nanowires. The translation of technology from a 14-transistor circuit to one with billions of transistors found on modern day microchips is no trivial task. Other major hurdles in the pursuit of bottom-up fabrication of integrated circuits will hopefully be overcome in time; this work marks one step in the long journey. In addition to microprocessors, semiconducting nanowire electronics have shown a great versatility, from solar cells and sensors to batteries and LEDs (19), all of which can stand to benefit from guided nanowire growth. This achievement of self-integration adds yet another inspiring tool in the expanding bag of tricks available to nanotechnologists.

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